ISO9001:2000 Certified SCI Quality System

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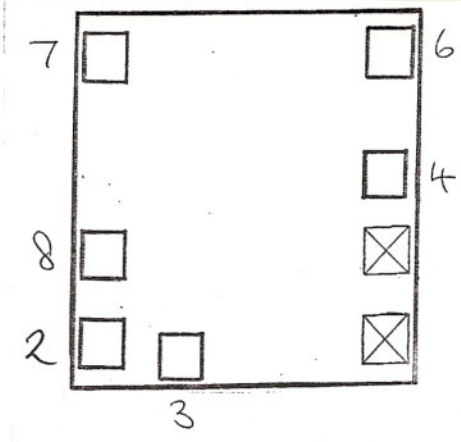
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

NOTE: Comlinear recommends that the chip back should be connected to $-V_{CC}$.



Pad	Function
1	NC
2	V_{inv}
3	$V_{non-inv}$
4	$-V_{CC}$
5	NC
6	V_{out}
7	$+V_{CC}$
8	R_p

E & O E. Dice can be supplied to this layout only if it forms part of a specification or the chip identification, if below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated above. If no potential is given the chip back should be isolated. Nominal metallisation thicknesses are based on manufacturer's information. 1 mil. = 0.001 inch. Tolerance ±3 mils.

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:	**DIE SIZE (Mils): 39 X 39**	**DATE: 3/16/00**
MFG: Comlinear	**THICKNESS:**	**P/N: CLD425ALC**